18. The circuit according to claim 15, wherein the digital data words have a length which varies in increments of 8 bits.

19. A multiplier unit for multiplying digital data words having a length which varies incrementally, the multiplier unit having a pipeline, the pipeline having a word length which is adjustable to match the length of the digital data words.

20. An arithmetic logic unit capable of performing arithmetic operations on digital data words having a length which varies incrementally, the arithmetic logic unit being adjustable to match the length of the digital data words.--

REMARKS

Applicant respectfully requests reconsideration and allowance of claims 1-20 which are pending in the above-identified application. Applicant has amended claims 1-14 and Applicant has added claims 15-20.

Applicant submits that the amendments made to claims 1-14 and the subject matter of new claims 15-20 are fully supported by the specification, claims and drawing as originally filed. Specifically, support for the amendments to claims 1-3 and 7-14 may be found in the claims as originally filed. Accordingly, no new matter has been added. Support for the amendments to claim 4 may be found at page 21, col. 1, paragraph 4 through col. 2, paragraph 2 and the sole figure on page 86 of the annexed IMAGINE DOCUMENTATION & USER MANUAL, Version 2.8, referenced in the specification as originally filed. Support for the amendments to claim 5 may be found in the sole figure on page 108 of the annexed IMAGINE DOCUMENTATION & USER MANUAL, Version 2.8, referenced in the specification as originally filed. Support for the amendments to claim 6 may be found at page 5, lines 27-36 of the originally filed specification.

The Examiner has indicated that a certified copy of the Dutch application has not been filed in the above-identified

application. Applicant will file a certified copy of the Dutch application in due course.

In paragraph 2 of the Office Action, the Examiner objected to the drawings under 37 CFR §1.84(f) because Figure 1 shows reference numeral "12" designating both a bus and a buffer. In paragraph 3 of the Office Action, the Examiner objected to the drawings under 37 CFR §1.84(f) because Figure 1 does not include reference numeral "4" as referred to in the specification. In response, Applicant has prepared a Request for Approval of Drawing Corrections which includes a proposed amendment to Figure 1 to reflect that the buffer is designated as "112" and to reflect bus "4" as referred to in the specification. Applicant submits that the Examiner's objection to the drawing under 37 CFR §1.84(f) would be overcome if approval of the drawing correction is obtained.

In response to the Examiner's objections to informalities in the specification (paragraph 4 of the Office Action), Applicant has amended the specification to reflect the changes suggested by the Examiner as well as other changes for clarity. Accordingly, Applicant submits that the Examiner's objection to the specification is overcome and should be withdrawn.

In paragraph 5 of the Office Action, the Examiner rejected claims 4-6, 8 and 12-14 under 35 U.S.C. § 112, second paragraph, for failing to particularly point out and distinctly claim the subject matter which the Applicant regards as the invention. The Examiner contends that claims 4-6 recite only functional statements and that claims 8 and 12-14 improperly recite "or other connections." In response, Applicant has amended claim 4 to recite that the multiplier includes a pipeline and a variable length accumulator to perform the specified function. Further, Applicant has amended claim 5 to recite that the ALU comprises a plurality of partitioned arithmetic logic units to perform the specified function. Still further, Applicant has amended claim 6 to recite that the shift register includes control logic to perform the specified function. Accordingly, claims 4-6 particularly point out and distinctly

claim the subject matter which the Applicant regards as the invention and, therefore, the Examiner's 35 U.S.C. Section 112, second paragraph, rejection of the subject claims should be withdrawn.

Further, Applicant has amended claims 8 and 12-14 to specifically include an instruction register and to recite that the transport of the integer data words from and to the multiplier unit, the arithmetic logic unit and the register unit is programmed from the instruction register. Applicant submits that the claimed apparatus of claims 8 and 12-14 includes only elements disclosed. Accordingly, claims 8 and 12-14 particularly point out and distinctly claim the subject matter which the Applicant regards as the invention and, therefore, the Examiner's 35 U.S.C. § 112, second paragraph, rejection of the subject claims should be withdrawn.

In paragraphs 6-7 of the Office Action, the Examiner rejected claim 6 under 35 U.S.C. §102(b) as being anticipated by United States Patent No. 4,931,971 to Cook. The Examiner contends that the Cook reference discloses an N-bit shifter/rotator as claimed. Applicant has amended claim 6 hereinabove to recite a shift register unit having control logic capable of receiving an integer data word having a length which is variable in increments of 8 bits. The Cook reference does not disclose a shift register having the elements as claimed by Applicant. Therefore, the Examiner's 35 U.S.C. §102(b) rejection of claim 6 cannot stand because anticipation of a claim can be found only if the prior art reference discloses every element of the claim. Ex parte Luck, 28 USPQ2d 1875, 1876 (Bd. App. 1993). Accordingly, Applicant respectfully requests that the Examiner's 35 U.S.C. §102(b) rejection of claim 6 be withdrawn.

In paragraphs 8-9 of the Office Action, the Examiner rejected claims 1-5 and 7-14 under 35 U.S.C. § 103 as being unpatentable over U.S. Patent No. 5,465,225 to Witte in view of U.S. Patent No. 4,901,267 to Birman. With reference to claims 1, 3, 4, 5, 8 and 13, the Examiner contends that the Birman reference discloses a multiplier unit, an arithmetic unit, register units and a supporting bus structure and the Witte

reference discloses that the arithmetic logic units may be adjusted to lengths less than the maximum length of each unit via masks. With reference to claims 2, 9 and 12, the Examiner contends that since the Birman reference discloses a three-step pipeline, the five-step pipeline recited in claims 2, 9 and 12 are obvious. With regard to claims 7 and 14, the Examiner contends that it would have been obvious to implement the circuit of Birman in integrated form. With regard to claim 10, the Examiner contends that it would have been obvious to use a five-step pipeline (in view of the three-step pipeline of Birman) and implement the circuit in integrated form. With regard to claim 11, the Examiner contends that it would have been obvious to implement the combined circuit of Birman and Witte in integrated form where the data words may be masked.

The present invention provides a circuit for processing data which uses a multiplier unit, an arithmetic logic unit, a register unit and a bus structure which are adjustable with respect to the length of the data word to be processed. Therefore, for example, the circuit of the present invention may process data words of 8 bits, 16 bits, 32 bits, etc.

The Witte reference discloses that mask bits (for example 1's or 0's) are added to a data word of lesser length than the arithmetic unit is designed to operate on (col. 1, line 44 through col. 2, line 18). As a result, the arithmetic logic unit, multiplier unit and register unit always operate on data words of the same length. Further, the Examiner admits that the disclosure of the Birman reference does not show the adjustable word length feature of claims 1 and 4-6. In contrast, the present invention provides a multiplier unit, an arithmetic logic unit, a register unit and a bus structure which are adjustable in accordance with the length of the data word to be processed.

Moreover, claim 1 as amended hereinabove recites that the bus structure has a plurality of separate buses, each bus having a register connected thereto. However, neither the Birman reference nor the Witte reference, taken alone or in combination, teach or suggest the bus structure as claimed by Applicant.

Neither the Birman reference nor the Witte reference taken alone or in combination teaches or suggests all of the elements as recited in amended claims 1 and 4-6 of the instant application and, accordingly, the Examiner's 35 U.S.C. § 103 rejection of claims 1 and 4-6 cannot stand and should be withdrawn. In re Royka, 490 F.2d 981 (CCPA 1974).

Further, claims 2, 3 and 7-14 depend on independent claim 1 and contain all of the limitations thereof. Therefore, Applicant submits that dependent claims 2, 3 and 7-14 recite likewise unique combinations at least for the reasons presented hereinabove with regard to the base claim.

Still further, new claim 15 provides a multiplier unit, an arithmetic logic unit, a register unit and a bus structure having a plurality of separate buses, each bus having a separate register connected thereto, where the structure is adjustable in accordance with the length of the data word to be processed. Therefore, in light of the arguments presented hereinabove with respect to claim 1, Applicant submits that new claim 15 is likewise patentable over the cited art.

Still further, new claims 16-18 depend on claim 15 and contain all of the limitations thereof. Therefore, Applicant submits that dependant claims 16-18 recite likewise unique combinations at least for the reasons presented hereinabove with regard to the base claim.

Still further, new claims 19 and 20 recite the feature that the digital data words, of the respective multiplier unit and arithmetic logic unit, are incrementally adjustable, which feature is not disclosed in the cited art of record. Therefore, new claims 19 and 20 are patentable over the prior art of record.

In light of the amendments made hereinabove, Applicant believes that the instant claims are in condition for allowance. The Examiner is invited to contact the undersigned to discuss any

still outstanding matters. Early and favorable action is earnestly solicited.

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner of Patents and Trademarks, Washington, D.C. 20231, on October 1, 1996:

James A. Finder
Name of applicant, assignee or Registered Representative

Signature

October 1, 1996
Date of Signature

Respectfully submitted,

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